

Mobile Intel® 915GM® Express Chipset

Development Kit User's Manual

March 2005

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Revision History

Date	Revision	Description
March 2005	001	Initial release of this document.

About This Manual 1

This user's manual describes the use of the Mobile Intel® 915GM® Express Chipset Development Kit. This manual has been written for OEMs, system evaluators, and embedded system developers. This document defines all jumpers, headers, LED functions, and their locations on the board, along with subsystem features and POST codes. This manual assumes basic familiarity in the fundamental concepts involved with installing and configuring hardware for a personal computer system.

For the latest information about the Mobile Intel® 915GM® Express Chipset Development Kit reference platform, visit:

http://developer.intel.com/design/intarch/devkits/index.htm

For design documents related to this platform, such as schematics and bill of materials, please contact your Intel Representative.

1.1 Content Overview

Chapter 1, "About This Manual" — This chapter contains a description of conventions used in this manual. The last few sections explain how to obtain literature and contact customer support.

Chapter 2, "Getting Started"— Provides complete instructions on how to configure the evaluation board and processor assembly by setting jumpers, connecting peripherals, providing power, and configuring the BIOS.

Chapter 3, "Theory of Operation" — This chapter provides information on the system design.

Chapter 4, "Hardware Reference"— This chapter provides a description of jumper settings and functions, board debug capabilities, and pinout information for connectors.

Appendix A, "Heat Sink Installation Instructions" gives detailed installation instructions for the 915GM Express Chipset heat sink.

1.2 Text Conventions

The following notations may be used throughout this manual.

#	The pound symbol (#) appended to a signal name indicates that the signal is active low.
Variables	Variables are shown in italics. Variables must be replaced with correct values.
Instructions	Instruction mnemonics are shown in uppercase. When you are programming, instructions are not case-sensitive. You may use either uppercase or lowercase.

Numbers

Hexadecimal numbers are represented by a string of hexadecimal digits followed by the character *H*. A zero prefix is added to numbers that begin with *A* through *F*. (For example, *FF* is shown as *0FFH*.) Decimal and binary numbers are represented by their customary notations. (That is, 255 is a decimal number and 1111 1111 is a binary number. In some cases, the letter *B* is added for clarity.)

Units of Measure

The following abbreviations are used to represent units of measure:

A	amps, amperes
GByte	gigabytes
KByte	kilobytes
Kohms	kilo-ohms
mA	milliamps, milliamperes
MByte	megabytes
MHz	megahertz
ms	milliseconds
mW	milliwatts
ns	nanoseconds
pF	picofarads
W	watts
V	volts
µA	microamps, microamperes
µF	microfarads
µs	microseconds
µW	microwatts

Signal Names

Signal names are shown in uppercase. When several signals share a common name, an individual signal is represented by the signal name followed by a number, while the group is represented by the signal name followed by a variable (*n*). For example, the lower chip-select signals are named CS0#, CS1#, CS2#, and so on; they are collectively called CS*n*#. A pound symbol (#) appended to a signal name identifies an active-low signal. Port pins are represented by the port abbreviation, a period, and the pin number (e.g., P1.0).

1.3 Glossary of Terms and Acronyms

This section defines conventions and terminology used throughout this document.

ADD2 — ADD2 is an acronym for Advanced Digital Display, 2nd Generation. ADD2 video interfaces come in two configurations: Normal and Reversed. The normal is often referred to as ADD2 or ADD2-N and the reversed is referred to as ADD2-R. The 915GM platform can only support the ADD2-R video interface.

Aggressor — A network that transmits a coupled signal to another network.

AGTL+ — The front-side bus uses a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain, and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.

Asynchronous GTL+ — The processor does not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output signals (FERR# and IERR#) and non-AGTL+ signals (THERMTRIP# and PROCHOT#) also utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to BCLK[1:0], and are therefore referred to as “Asynchronous GTL+ Signals”. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two BCLKs in order for the processor to recognize them.

Bus Agent — A component or group of components that, when combined, represent a single load on the AGTL+ bus.

Crosstalk — The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks.

- Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor’s signal.
- Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor’s signal.
- Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching.
- Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.

Flight Time — Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the TCO of the driver,

plus any adjustments to the signal at the receiver needed to ensure the setup time of the receiver. More precisely, flight time is defined as:

- The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings.
- Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance, and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects.
- Maximum flight time is the largest acceptable flight time a network will experience under all conditions.
- Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.

IrDA IrDA is an acronym for Infrared Data Association, and this association has outlined a specification for serial communication between two devices via a bi-directional infrared data port. The 915GM platform has such a port and it is located on the rear of the platform between the two USB connectors.

ISI Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI may impact both timing and signal integrity.

Network The network is the trace of a Printed Circuit Board (PCB) that completes an electrical connection between two or more components.

Overshoot The maximum voltage observed for a signal at the device pad, measured with respect to VCC.

Pad The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.

Pin The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings may be measured at the pin.

Power-Good "Power-Good," "PWRGOOD," or "CPUPWRGOOD" (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.

Ringback — The voltage to which a signal changes after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.

System Bus — The System Bus is the microprocessor bus of the processor.

Setup Window — The time between the beginning of Setup to Clock (TSU_MIN) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.

SSO — Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay ("push-out") or a decrease in propagation delay ("pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.

Stub — The branch from the bus trunk terminating at the pad of an agent.

Trunk — The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.

Undershoot — The minimum voltage extending below VSS observed for a signal at the device pad.

V_{CC} (CPU core) — V_{CC} (CPU core) is the core power for the processor. The system bus is terminated to V_{CC} (CPU core).

Victim — A network that receives a coupled crosstalk signal from another network is called the victim network.

VRD 10.0 — The Voltage Regulator Module (a down on the board solution) specification for the Intel® Pentium® 4 Processor with HT Technology processor. It is a DC-DC converter module that supplies the required voltage and current to a single processor.

Table 1 defines the acronyms used throughout this document.

Table 1. Acronyms (Sheet 1 of 2)

Acronym	Definition
AC	Audio Codec
ASF	Alert Standard Format
AMC	Audio/Modem Codec.
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
CMC	Common Mode Choke
CNR	Communications and Networking Riser
EMI	Electro Magnetic Interference
ESD	Electrostatic Discharge

Table 1. Acronyms (Sheet 2 of 2)

Acronym	Definition
FS	Full-speed. Refers to USB
HS	High-speed. Refers to USB
ICH	I/O Controller Hub
LOM	LAN on Motherboard
LPC	Low Pin Count
LS	Low-speed. Refers to USB
MC	Modem Codec
PCM	Pulse Code Modulation
PLC	Platform LAN Connect
RTC	Real Time Clock
SATA	Serial ATA
SMBus	System Management Bus. A two-wire interface through which various system components may communicate.
SPD	Serial Presence Detect
STR	Suspend To RAM
TCO	Total Cost of Ownership
TDM	Time Division Multiplexed
TDR	Time Domain Reflectometry
µBGA	Micro Ball Grid Array
USB	Universal Serial Bus

1.4 Support Options

1.4.1 Electronic Support Systems

Intel's web site (http://www.intel.com/) provides up-to-date technical information and product support. This information is available 24 hours per day, 7 days per week, providing technical information whenever you need it.

Product documentation is provided online in a variety of web-friendly formats at:

http://appzone.intel.com/literature/index.asp

1.4.2 Additional Technical Support

If you require additional technical support, please contact your Intel Representative or local distributor.

1.5 Product Literature

You can order product literature from the following Intel literature centers:

Table 2. Intel Literature Centers

Location	Telephone Number
U.S. and Canada	1-800-548-4725
U.S. (from overseas)	708-296-9333
Europe (U.K.)	44(0)1793-431155
Germany	44(0)1793-421333
France	44(0)1793-421777
Japan (fax only)	81(0)120-47-88-32

1.6 Related Documents

The table below provides a summary of publicly available documents related to this development kit. As supplements to the documents listed below, technical white papers detailing specific features of the 915GM Express Chipset can be found at:

http://developer.intel.com/design/chipsets/915Gm/index.htm

For any additional documentation, please contact your Intel Representative.

Table 3. Related Documents (Sheet 1 of 2)

Document Title	Order Number
Intel® Pentium® M Processor on 90nm Process with 2 MByte L2 Cache Datasheet	302189
Intel® Pentium® M Processor on 90nm Process with 2 MByte L2 Cache Specification Update	302209
Intel® Pentium® M Processor on 90 nm Process with 2 MByte L2 Cache for Embedded Applications Thermal Design Guide	302231
Intel® Celeron® M Processor on 90nm Process Datasheet	303110
Intel® Celeron® M Processors Specification Update	300302
Intel® Pentium® M Processor and Intel® Celeron® M Processor for Embedded Applications Thermal Design Guide	273885
Enhanced Intel® SpeedStep® Technology for the Intel® Pentium® M Processor	301174
Intel® Architecture Software Developer's Manual: • IA-32 Intel® Architecture Software Developer's Manual Volume 1: Basic Architecture • IA-32 Intel® Architecture Software Developer's Manual Volume 2A: Instruction Set Reference Manual A-M • IA-32 Intel® Architecture Software Developer's Manual Volume 2B: Instruction Set Reference Manual N-Z • IA-32 Intel® Architecture Software Developer's Manual Volume 3: System Programming Guide	 253665 253666 253667 253668
IA-32 Intel® Architecture Optimization Reference Manual	248966
Mobile Intel® 915PM/GM/GMS and 910GML Express Chipset Datasheet	305264

Table 3. Related Documents (Sheet 2 of 2)

Intel® 915GM Express Chipset GMCH Thermal Design Guide for Embedded Applications	16566†
Intel® I/O Controller Hub 6 (ICH6) Family Datasheet	301473
Intel® I/O Controller Hub 6 (ICH6) Family Specification Update	301474
Intel® I/O Controller Hub 6 (ICH6) Family Thermal Design Guide	302362
LPC Slot and Sideband Header Specification	14159†

†Contact your Intel representative for access to this document.

Getting Started 2

This chapter identifies the evaluation kit's key components, features and specifications. It also details basic board setup and operation.

2.1 Overview

The evaluation board consists of a baseboard populated with the Intel® 915GM® Express Chipset Development Kit, other system board components, and peripheral connectors.

Note: The evaluation board is shipped as an open system allowing for maximum flexibility in changing hardware configuration and peripherals. Since the board is not in a protective chassis, take extra precaution when handling and operating the system.

2.1.1 Intel® 915GM® Express Chipset Development Kit Features

Features of the development kit board are summarized below:

Processor

- Supports Intel® Pentium® M Processor with 2 MByte L2 Cache on 90 nm process in the 478 pin Flip Chip Pin Grid Array (Micro-FCPGA) package
 - — Supported processors are the Intel® Pentium® M 760 Processor and the Intel® Pentium® M 738 Processor
- Supports Intel® Celeron® M Processor on 90 nm process in the 478 pin Flip Chip Pin Grid Array (Micro-FCPGA) package
 - — Supported processors are the Intel® Celeron® M 370 Processor and the Intel® Celeron® M 373 Processor

Note: This reference platform does not support the Intel® Pentium® M 745 Processor.

Mobile Intel® 915GM Express Graphics Memory Controller Hub (915GM Express GMCH)

- 1257 pin Micro-FCBGA Package
- Supports a 400/533 MHz front side bus
- Dual-Channel DDR2 at 400/533 MHz
- Two SODIMM slots (one per channel) support DDR2 SODIMMS (unbuffered, non-ECC) modules
- Supports 128 MBytes to 2 GBytes using 256 Mbit, 512 Mbit, or 1 Gbit technology
- x16 PCI Express Graphics or Serial Digital Video Out (SDVO) port
- LVDS, VGA & S-Video video support

I/O Controller Hub 6 (ICH6-M)

- 609 pin plastic BGA package
- DMI (x4) interface with GMCH
- Two SATA and one IDE (40 pin) Hard Drive interface
- Two PCI 2.3 compliant desktop slots
- 82802AC8 Firmware Hub (FWH)
- 82562EZ 10/100 Mbps Platform LAN Connect (PLC)
- Two x1 PCI Express slots.

Note: There are actually three x1 PCI Express slots but slot 2 was used for validation purposes. Only slots 0 and 1 are supported.

Clocking

- CK-410M and CK-SSCD
- Battery-backed real time clock

Connector Interface Summary

- One x16 PCI Express Video Interface, doubles as an ADD2-R connector to provide access to dual SDVO ports if PCI Express is unused
- Two SATA ports
- One Ultra ATA (33/66/100/133) IDE connector supporting up to two IDE devices
- Eight Universal Serial Bus (USB) 2.0 ports (Five ports provided on rear-panel, two provided via front-panel header (J6H2), and one at the PCI Express docking connector.)
- Two PCI 2.3 compliant 33 MHz interface connectors
- PS/2-style keyboard and PS/2 mouse (6-pin mini-DIN) connectors
- Standard S-Video connector at back panel interface
- LVDS connector on top of circuit board near GMCH
- One VGA connector provides access to integrated graphics
- One LAN connector providing 10/100 connectivity from Intel 82562EZ 10/100 Mbit PLC
- One 9-pin serial port connector.
- One IrDA port
- Two PCI Express slots (x1)
- Two SODIMM connectors on rear side of circuit board

Debug Features

- Extended Debug Port (XDP) connector
- On-board Port 80h display

Miscellaneous Features

- Configurable for ATX 1.1 Power Supply in desktop mode or AC Mobile Brick/Battery Pack for Mobile Mode
- ATX Form Factor eight layer PCB

- AMI* system BIOS
- Built-in Wake On LAN (WOL) header
- Three built-in fan power connectors: Rear Chassis Fan, CPU Fan, Front Chassis Fan
- Power/Reset buttons
- CMOS clear jumper
- BIOS recovery jumper
- Boot Block protection jumper
- Support for Serial, IrDA, serial mouse, and keyboard

2.2 Included Hardware and Documentation

The following hardware and documentation is included in the development kit:

- One Intel® 915GM® Express Chipset Development Kit board
- One Intel® Pentium M® Processor with 2 MB L2 Cache on 90 nm process in the 478 pin Flip-Chip Pin Grid Array (Micro-FCPGA) package (Installed)
- One Firmware Hub (FWH) (Installed)
- One MCH (915GM) heat sink (Installed)
- One Type 2032, socketed 3 V lithium coin cell battery (Installed)
- One128 MByte DDR2 SODIMM (200 Pin)
- One CPU thermal solution and CPU back plate (included in kit box – not populated on board)
- One power supply block and cable
- One laptop to desktop IDE adaptor
- One 2.5 inch IDE hard drive
- One cable kit

2.3 Software Key Features

The software in the kit was chosen to facilitate development of real-time applications based on the components used in the evaluation board. The driver CD included in the kit contains all of the software drivers necessary for basic system functionality under the following operating systems: Windows* 2000/XP/XP Embedded, and Linux*.

Note: While every care was taken to ensure the latest versions of drivers were provided on the enclosed CD at time of publication, newer revisions may be available. Updated drivers for Intel components can be found at: http://www.intel.com.

For all third-party components, please contact the appropriate vendor for updated drivers.

Note: Software in the kit is provided free by the vendor and is only licensed for evaluation purposes. Refer to the documentation in your evaluation kit for further details on any terms and conditions

that may be applicable to the granted licenses. Customers using the tools that work with Microsoft* products must license those products. Any targets created by those tools should also have appropriate licenses. Software included in the kit is subject to change.

Refer to http://developer.intel.com/design/intarch/devkits for details on additional software from other third-party vendors.

2.3.1 AMI* BIOS

This development kit ships pre-installed with AMI* BIOS pre-boot firmware from AMI*. AMI* BIOS provides an industry-standard BIOS platform to run most standard operating systems, including Windows* 2000/XP/XP Embedded, Linux*, and others.

The AMI* BIOS Application Kit (available through AMI*) includes complete source code, a reference manual, and a Windows-based expert system, BIOStart*, to enable easy and rapid configuration of customized firmware for your Mobile Intel® 915GM® Express Chipset .

The following features of AMI* BIOS are enabled in the Mobile Intel® 915GM® Express Chipset :

- DDR2 SDRAM detection, configuration, and initialization
- 915GM Express Chipset configuration
- POST codes displayed to port 80h
- PCI/PCI Express device enumeration and configuration
- Integrated video configuration and initialization
- Super I/O configuration
- CPU microcode update

2.4 Before You Begin

Additional hardware may be necessary to successfully set up and operate the evaluation board.

VGA Monitor: Any standard VGA or multi-resolution monitor may be used. The setup instructions in this chapter assume the use of a standard VGA monitor, TV, or flat panel monitor.

Keyboard: The evaluation board can support either a PS/2 or USB style keyboard.

Mouse: The evaluation board can support either a PS/2 or USB style mouse.

Hard Drives and Compact Disc Drives: Up to two SATA drives and two IDE devices (master and slave) may be connected to the evaluation board. A compact disc drive may be used to load the OS. All these storage devices maybe attached to the board simultaneously.

Video Adapter: Integrated video is provided on the back panel of the evaluation board. Alternately, a standard PCI Express video adapter or an ADD2-R video adapter may be used for additional display flexibility. Please contact the respective vendors for drivers and necessary software for adapters not provided with this development kit. Check the BIOS for the proper video settings. See Section 2.6, “Configuring the BIOS” on page 21 for more information.

Note: The enclosed driver CD includes drivers necessary for LAN, Integrated graphics, and system INF utilities.

Network Adapter: A 10/100 Mbit network interface is provided on the evaluation board. The network interface will not be operational until after all the necessary drivers have been installed. A standard PCI/PCI Express adapter may be used in conjunction with, or in place of, the onboard network adapter. Please contact the respective vendors for drivers and necessary software for adapters not provided with this development kit.

You must supply appropriate network cables to utilize the LAN connector or any other installed network cards.

Power Supply: The 915GM Express Chipset has the option to be powered from two different power sources: an ATX power supply, or 'Mobile Brick'. The 915GM Express Chipset contains all of the voltage regulators necessary to power the system.

There are two main supported power supply configurations, Desktop and Mobile. The Desktop solution consists of only using the ATX power supply. The Mobile solution consists of only using the AC Brick.

Note: Desktop peripherals, including add-in cards, will not work in mobile power mode. If desktop peripherals are used, the platform must be powered using desktop power mode. The AC Brick power supply configuration does not provide the 12 V supply required by most desktop peripherals.

Note: Use an "ATX12V" 1.1 Spec compliant power supply regardless of vendor or wattage level (an "ATX12V" rating means V5 min current =0.1 A, "ATX" V5 min current = 1.0 A, among other differences). For example, the Sparkle Model No. FSP250-60BT meets this requirement and is an ATX12V 1.1 Spec compliant power supply. For more information, see http://www.formfactors.org/developer/specs/atx/atxspecs.htm.

Note: If the power button on the ATX power supply is used to shut down the system, wait at least five seconds before turning the system on again to avoid damaging the system.

Other Devices and Adapters: The evaluation board functions much like a standard desktop computer motherboard. Most PC-compatible peripherals can be attached and configured to work with the evaluation board.

2.5 Setting Up the Evaluation Board

Once the necessary hardware (described in Section 2.4) has been gathered, follow the steps below to set up the 915GM Express Chipset evaluation board.

Note: To locate items discussed in the procedure below, please refer to Section 4.

1. Create a safe work environment.

 Ensure a static-free work environment before removing any components from their anti-static packaging. The evaluation board is susceptible to electrostatic discharge damage, and such damage may cause product failure or unpredictable operation.

2. Inspect the contents of your kit.

 Check for damage that may have occurred during shipment. Contact your sales representative if any items are missing or damaged.

Caution: ***Connecting the wrong cable or reversing the cable can damage the evaluation board may damage the device being connected. Since the board is not in a protective chassis, use caution when connecting cables to this product.***

Caution: ***Standby voltage is constantly applied to the board. Therefore, do not insert or remove any hardware unless the system is unplugged.***

Note: The evaluation board is a standard ATX form factor. An ATX chassis may be used if a protected environment is desired.

3. Check the jumper default position setting. Refer to Figure 4 for jumper location. Jumper J6H1 is used to clear the CMOS memory. Make sure this jumper is set for normal operation.
4. Be sure to populate the following hardware on your evaluation board:
 - — One Pentium® M 760 Processor
 - — One processor thermal solution
 - — One 128 MByte DDR2 533 SODIMM (200-pin)

Note: For proper installation of the CPU thermal solution, please refer to Appendix A, "Heat Sink Installation Instructions"

5. Install a SATA or IDE hard disk drive.
6. Connect any additional storage devices to the evaluation board.
7. Connect the keyboard and mouse.

 Connect a PS/2-style or USB mouse and keyboard (see Figure 3 on page 38 for connector locations).

Note: J1A1 (on the baseboard) is a stacked PS/2 connector. The bottom connector is for the keyboard and the top is for the mouse.

8. Connect an Ethernet cable (optional).
9. Connect the monitor through the VGA connector.
10. Connect the power supply.

 Connect an appropriate power supply to the evaluation board. Make sure the power supply is not plugged into an electrical outlet (turned off). After connecting the power supply board connectors, plug the power supply cord into an electrical outlet.
11. Power up the board.

 Reset and Power are implemented on the evaluation board through buttons located on SW1C1and SW1C2, respectively. Refer to Figure 5 on page 42 for switch locations.

 Turn on the power to the monitor and evaluation board. Ensure that the fansink on the processor is operating.
12. Install operating system and necessary drivers

 Depending on the operating system chosen, all necessary drivers for components included in this development kit can be found on the enclosed CD. Please see Section 2.3 for information on obtaining updated drivers.

2.6 Configuring the BIOS

AMI* BIOS is pre-loaded on the evaluation board. The default BIOS settings may need to be modified to enable/disable various features of the evaluation board. The setup program can be used to modify BIOS settings and can be accessed during the Power On Self Test (POST). Setup options are configured through a menu-driven user interface. For AMI BIOS POST codes, visit:

http://www.ami.com

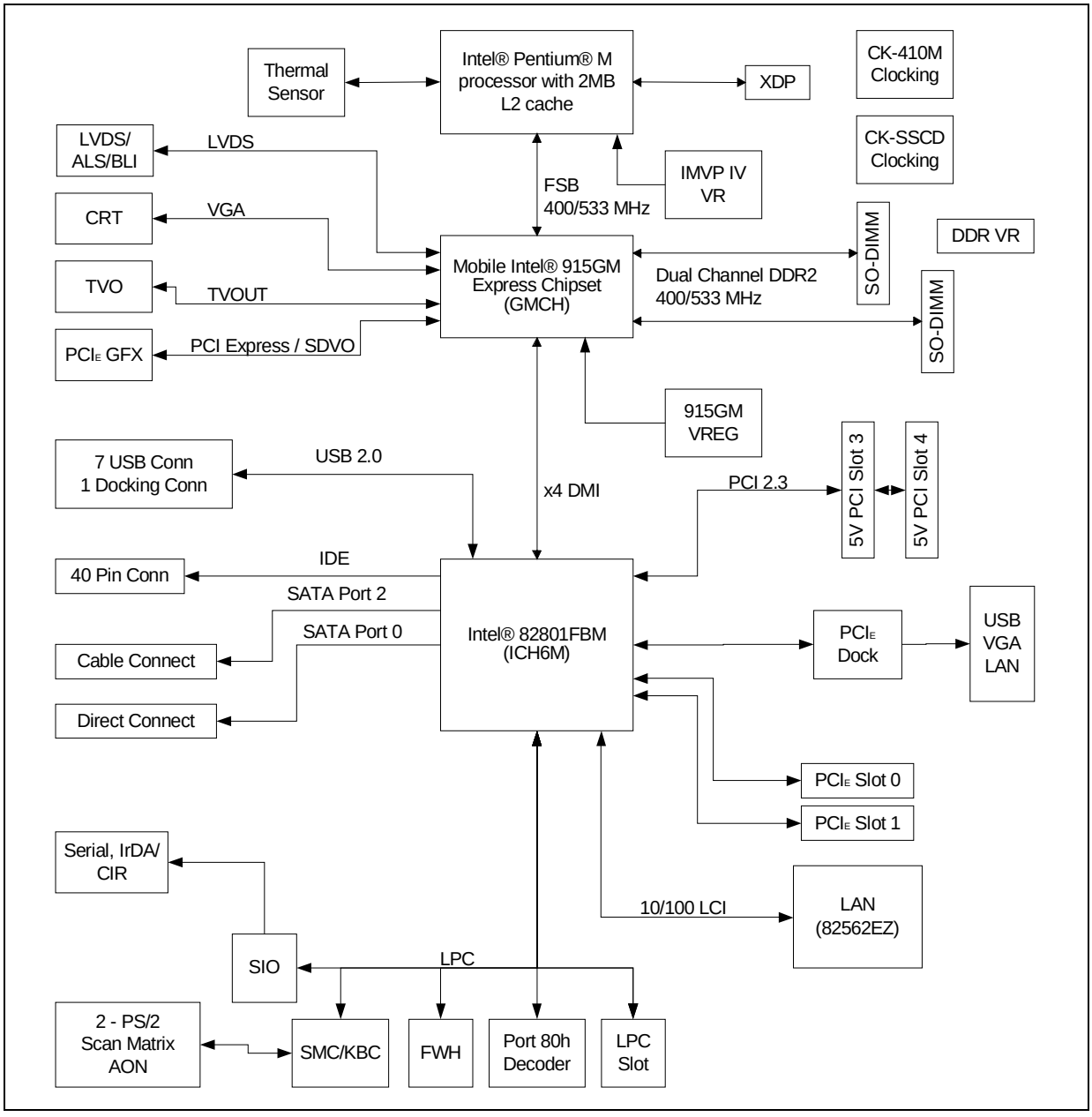
BIOS updates periodically may be posted to Intel's Developers' Web site at:

http://developer.intel.com/design/intarch/devkits/

Theory of Operation 3

3.1 Block Diagram

Figure 1. Intel® 915GM® Express Chipset Development Kit Block Diagram



3.2 Mechanical Form Factor

The evaluation board conforms to the ATX form factor. For extra protection in a development environment, you may want to install the evaluation board in an ATX chassis. Internal and rear panel system I/O connectors are described in Section 3.4.3. An overview of connector and slot locations is provided in Section 4.

3.3 Thermal Management

The objective of thermal management is to ensure that the temperature of each component is maintained within specified functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements.

Operation outside the functional limit can degrade system performance and cause reliability problems.

The development kit is shipped with a fansink thermal solution for installation on the processor. This thermal solution has been tested in an open-air environment at room temperature and is sufficient for evaluation purposes. The designer must ensure that adequate thermal management is provided for any customer-derived designs.

3.4 System Features and Operation

The following sections provide a detailed view of system features and operation. Refer to Figure 2 and Table 7 for the location of the major components of the platform.

3.4.1 Intel® 915GM® Express Chipset Development Kit

The 915GM Express Chipset features the 915GMCH and the Intel® I/O Controller Hub (ICH6-M) chipset.

The 915GM Express Chipset GMCH provides the processor interface optimized for Intel® Pentium® M Processors, system memory interface, DMI and internal graphics. It provides flexibility and scalability in graphics and memory subsystem performance. The following sections describe the reference board's implementation of the 915GM Express Chipset GMCH features.

- 1257 Micro-FCBGA package
- 400/533MHz Front Side Bus
- 32-bit host bus addressing
- System memory controller (DDR2 implemented)
 - — Supports Dual Channel and Single Channel operation
 - — Two 200-pin SODIMM slots
 - — DDR2 400/533
- Direct Media Interface (DMI)
- Integrated graphics based on Intel's Graphics Media Accelerator 900

- — Directly supports on-board VGA, S-Video and LVDS interfaces.
- — Supports resolutions up to 2048 x 1536 @ 85 Hz.

- SDVO interface via PCI Express x16 connector provides maximum display flexibility
 - — Can drive up to two display outputs
 - — Maximum single channel resolution of 2048 x 1536 @ 60 Hz

3.4.1.1 System Memory

The evaluation board supports DDR2 400/533 main memory. Two 200-pin SODIMM connectors (one per channel) on the board support unbuffered, non-ECC, single and double-sided DDR2 400/533 MHz SODIMMs. These SODIMMs provide the ability to use up to 1 Gbit technology for a maximum of 2 GBytes system memory.

Note: Memory that utilizes 128 MBit technology is not supported by the GMCH and is not supported on the 915GM Express Chipset.

Note: The SODIMM connectors are on the back side of the board.

Caution: Standby voltage is applied to the SODIMM sockets when the system is in the S3 state. Therefore, do not insert or remove SODIMMs unless the system is unplugged.

3.4.1.2 DMI

The 915GM Express Chipset GMCH's Direct Media Interface (DMI) provides high-speed bi-directional chip-to-chip interconnect for communication with the ICH6-M.

3.4.1.3 Advanced Graphics and Display Interface

The reference board has five options for displaying video, VGA, LVDS, TVOUT, SDVO, or PCI Express Graphics. SDVO (ADD2-R) and PCI Express Graphics are multiplexed on the same pins within the 915GM Express Chipset. The 915GM Express Chipset contains one SDVO/PCI Express Graphics Slot (J6C1) for a PCI Express compatible graphics card or an SDVO compatible graphics card, one LVDS connector (J5F1), one TVOUT connector (J1A1), and one 15-pin VGA connector (J2A1B).

3.4.2 ICH6-M

The ICH6-M is a highly integrated multifunctional I/O controller hub that provides the interface to the system peripherals and integrates many of the functions needed in today's PC platforms. The following sections describe the reference board implementation of the ICH6-M features, which are listed below:

- Two PCI Express (x1) connectors
- Two PCI connectors
- LPC interface
- Wake-On-LAN support
- System management

- ACPI* 2.0 compliant
- Real Time Clock
- 609 mBGA package
- Two SATA drive connectors
- One IDE connector
- Eight Universal Serial Bus (USB) 2.0 ports (five ports provided on rear-panel, two provided via front-panel header (J6H2) and one at the PCI Express docking connector.)
- Integrated 10/100 MAC

3.4.2.1 PCI Express Slots

The reference board has two PCI Express slots for add-in cards. The PCI Express interface is compliant to the *PCI Express Rev. 01a Specification*.

3.4.2.2 PCI Slots

The reference board has two x1 PCI slots for add-in cards. The PCI bus is compliant to the PCI Rev. 2.3 Specification at 33 MHz.

3.4.2.3 On-Board LAN

The 82562EZ provides the PHY for the Intel ICH6-M's integrated LAN connect interface. This provides a low cost, reduced footprint solution for 10/100 Mbit LAN connectivity. The 82562EZ component is connected to the ICH6-M chipset through the LAN Connect Interface (LCI) and to an RJ45 connector at J5A1A with built in magnetic decoupling. Access to this interface is provided on the rear I/O panel (See Figure 3 on page 38).

Features of the 82562EZ are as follows:

- IEEE* 802.3 10BASE-T/100BASE-TX compliant physical layer interface
- IEEE 802.3u Auto-Negotiation support
- Digital Adaptive Equalization control
- Link status interrupt capability
- XOR Tree mode support for board testing
- Three-port LED support (speed, link, and activity)
- 10BASE-T auto-polarity correction
- Platform LAN connect interface support
- 82540EM layout compatible
- Diagnostic loopback mode
- 1:1 transmit transformer ratio support
- Low power (less than 300 mW in active transmit mode)
- Reduced power in "unplugged mode" (less than 50 mW)
- Automatic detection of "unplugged mode"

3.4.2.4 AC'97 and High Definition Audio

AC'97 and High Definition Audio are not supported on the board.

3.4.2.5 ATA / Storage

The 915GM Express Chipset provides one parallel ATA IDE connector and two serial ATA connectors. The parallel ATA IDE Connector is a standard 40-pin 0.1" center header at J7J2 for a desktop IDE drive. A power connector is supplied on the 915GM Express Chipset to power a parallel ATA hard disk drive at J4J2. One of the two serial ATA connectors on the 915GM Express Chipset is a direct connect connector; located at J8J3. The other serial ATA connector is broken up into two connectors. One connector is for the serial data signals, and the other is for to power the serial ATA hard disk drive. These connectors are located at J7H1 and J6H3. A green LED at CR7J1 indicates activity on ATA channel.

The 915GM Express Chipset also supports 'ATA swap' capability for both the parallel IDE channel and the serial ATA channels. The parallel IDE device should be powered from the power connector, J4J2, on the 915GM Express Chipset to utilize the hot swap feature. This feature requires customer-developed software support.

3.4.2.6 USB Connectors

The ICH6-M provides a total of eight USB 2.0 ports. Three ports are routed to a triple-stack USB connector at J3A1. Two ports are routed to a combination RJ-45/dual USB connector at J5A1B. Two ports are routed to a USB front panel header at J6H2. The final USB port is routed to the PCI Express Docking Connector at J9J4.

3.4.2.7 LPC Super I/O (SIO)/LPC Slot

An SMSC LPC47N207 serves as the SIO on the 915GM Express Chipset platform. Shunting the jumper at J7E4 to the 2-3 positions can disable the SIO by holding it in reset. This allows other SIO solutions to be tested in the LPC slot at J8F2. A sideband header is provided at J9G2 for this purpose. This sideband header also has signals for LPC power management. Information on this header is on sheet 29 of the 915GM Express Chipset schematics and is detailed in the "LPC Slot and Sideband Header Specification" (see Table 3, "Related Documents" on page 13).

3.4.2.8 Serial, IrDA

The SMSC SIO incorporates a serial port, and IrDA (Infrared), as well as general purpose IOs (GPIO). The serial port connector is provided at J2A1A, and the IrDA transceiver is located at U4A2. The IrDA transceiver on 915GM Express Chipset supports both SIR (slow IR) and CIR (Consumer IR). The option to select between the two is supported through software and GPIO pin on the SIO.

3.4.2.9 BIOS Firmware Hub (FWH)

The 8 Mbit Flash device used on the 915GM Express Chipset to store system and video BIOS as well as an Intel Random Number Generator (RNG) is a socketed E82802AC8 a 32-pin PLCC package. The reference designator location of the FWH device is U8G1. The BIOS can be upgraded using an MS-DOS* based utility and is addressable on the LPC bus off of the ICH6-M.

3.4.2.10 System Management Controller (SMC)/Keyboard Controller

The Hitachi* H8S/HD64F2 serves as both SMC and KBC for the platform. The SMC/KBC controller supports two PS/2 ports, battery monitoring and charging, EMA support, wake/runtime SCI events, and power sequencing control. The two PS/2 ports on the 915GM Express Chipset are for legacy keyboard and mouse. The keyboard plugs into the bottom jack and the mouse plugs into the top jack at J1A2. Scan matrix keyboards can be supported via an optional connector at J9E2.

3.4.2.11 Clocks

The 915GM Express Chipset board uses a CK-410M and CK-SSCD compatible solution. The CK-SSCD solution offers improved EMI performance by spreading the radiated clock emissions over a wider spectrum than a single frequency. This is accomplished while controlling the clock frequency deviation such that system performance is not compromised. The FSB frequency is determined from decoding the processor BSEL settings.

3.4.2.12 Real Time Clock

An on-board battery at BT5H1 maintains power to the real time clock (RTC) when in a mechanical off state. A CR2032 battery is installed on the 915GM Express Chipset development kit.

3.4.2.13 Thermal Monitoring

The processor has a thermal diode for temperature monitoring. The SMC thermal monitoring device will throttle the processor if it becomes hot. If the temperature of the processor rises too high, the SMC will alternately blink the CAPS lock and NUM lock LEDs on the board, and the board will shut down.

3.4.3 System I/O and Connector Summary

The evaluation board provides extensive I/O capability in the form of internal connectors and headers as detailed by the following list. For detailed information on these connectors and headers, please refer to “Hardware Reference” on page 36.

- One (x16) PCI Express connector
- Two (x1) PCI Express connectors
- Two PCI connectors
- One IDE interface (supports two drives)
- Two SATA connectors
- Two USB ports via front panel header (J8G1)
- One LVDS video connector

In addition to the internal I/O connections listed above, the evaluation board also contains the following I/O on the rear panel (as illustrated in Figure 3 on page 38).

- Five USB ports on back panel.
- VGA connector
- PS/2-style keyboard and mouse ports
- LAN connector
- One 9-pin serial connector
- One IrDA port
- One SVideo connector

3.4.3.1 PCI Express Support

The evaluation board provides access to one x16 PCI Express connector. Any industry standard x16 PCI Express video adapter may be used with this interface. The evaluation board also provides access to two x1 PCI Express connectors. Any industry standard x1 PCI Express adapter may be used with these interfaces.

3.4.3.2 SATA Support

The evaluation board provides support for up to two SATA disk drives. The SATA controllers are software compatible with IDE interfaces, while providing lower pin counts and higher performance.

3.4.3.3 IDE Support

The evaluation board has a 40-pin connector for the ICH6-M's integrated IDE controller. This connector supports up to two Ultra ATA/100 hard drives; one master and one slave.

3.4.3.4 USB Ports

The evaluation board provides eight USB (2.0) ports on the rear panel and two additional ports through the front panel header. (J8G1).

There are four UHCI Host Controllers and two EHCI Host Controllers. Each UHCI Host Controller includes a root hub with two separate USB ports each, for a total of eight legacy USB ports.

Each EHCI Host Controllers includes a root hub that supports up to four USB 2.0 ports. The connection to either the UHCI or EHCI controllers is dynamic and dependant on the particular USB device. As such, all ports support High Speed, Full Speed, and Low Speed (HS/FS/LS).

3.4.3.5 VGA Connector

A standard 15 pin D-Sub connector on the rear panel provides access to the analog output of the Intel GMA 900. The integrated graphics supports a maximum resolution of 2048 x 1536 @ 85Hz. This can be connected to any capable analog CRT or flat panel display with analog input.

When used in conjunction with any of the other display options, the displays can operate Dual Independent mode. This allows the unique content to appear on each display at unique refresh rates and timings.

3.4.3.6 Keyboard/Mouse

The keyboard and mouse connectors are PS/2 style, six-pin stacked miniature DSUB connectors. The top connector is for the mouse and the bottom connector is for the keyboard.

3.4.3.7 32 bit/33 MHz PCI Connectors

Two industry standard 32 bit/33 MHz PCI connectors are provided on the evaluation board. These slots support 3.3 V and 5 V devices.

3.4.3.8 Ethernet 10/100 LAN Interface connector

The evaluation board provides support for one Industry standard 10/100 RJ45 LAN Interface Connector (Integrated with the dual USB connector).

3.4.3.9 LVDS Flat Panel Display Interface

The evaluation board provides support for one forty-four pin LVDS video interface connector. The provided LVDS connects to most flat panel display assemblies.

3.4.4 Post Code Debugger

A port 80-83 display at CR6A1, CR6A2, CR6A3, and CR6A4 show cycles and can be used for debug information during POST. The evaluation board uses an AMI* BIOS.

For AMI* BIOS POST codes, please visit: http://www.ami.com

3.5 Clock Generation

The 915GM Express Chipset board uses a CK-410M and CK-SSCD compatible solution. The FSB frequency is determined from decoding the processor BSEL settings.

The clock generator provides Processor, GMCH, ICH6-M, PCI, PCI Express, SATA, and USB reference clocks. Clocking for DDR2 is provided by the GMCH.

Table 4. System Clocks (Sheet 1 of 2)

Clock Name	Speed
CPU	133 MHz @ 533 100 MHz @ 400
DDR2	100 MHz @ 400 133 MHz @ 533
PCI Express and DMI	100 MHz
SATA	100 MHz

Table 4. System Clocks (Sheet 2 of 2)

Clock Name	Speed
PCI	33 MHz
Audio	14 MHz
USB	48 MHz

3.6 Power Management States

The evaluation board supports S1 (Stop Grant), S3 (Suspend to RAM), S4 (Suspend to disk), and S5 (Soft-off) states. Transition requirements are detailed below.

Table 5 lists the power management states that have been identified for the 915GM Express Chipset Platform.

Table 5. Intel® 915GM® Express Chipset Development Kit Power Management States

State	Description
G0/S0/C0	Full On
G0/S0/C2	STPCLK# signal active
G0/S0/C3	Deep Sleep: DPSLP# signal active
G0/S0/C4	Deeper Sleep: DPRSLP# signal active
G1/S3_HOT	Suspend to RAM (all S3 rails are turned on except processor power rails)
G1/S3_COLD	Suspend to RAM (all S3 rails are turned off)
G1/S4	Suspend to Disk
G2/S5	Soft Off
G3	Mechanical Off

3.6.1 Transition to S1 or S3

If enabled, the transition to S1 or S3 from the full-on state can be accomplished in the following ways:

- The OS performs the transition through software.
- Press the front panel power button for less than four seconds (assuming the OS power management support has been enabled).

3.6.2 Transition to S4

“Wake on S4” (Suspend to disk) is controlled by the operating system.

3.6.3 Transition to S5

The transition to S5 is accomplished by the following means:

- Press the front panel power button for less than four seconds (if enabled through the OS).

- Press the front panel power button for more than four seconds to activate power button override.

3.6.4 Transition to Full-On

The transition to the Full-On state can be from S1, S3, or S5. The transition from S1 or S3 is a low latency transition that is triggered by one of the following wake events:

- Power management timer expiration
- Real Time Clock (RTC) triggered alarm
- Power button activation
- USB device interrupt
- PME# assertion
- Mouse/Keyboard movement (Applies only to S1 Transition)
- AC power loss

For AC power loss, the system operation is defined by register settings in the Intel ICH6-M. Upon the return of power, a BIOS option, set prior to the power loss, allows the system to either go immediately to the S5 state, or reboot to the Full-On state, no matter what the state was before the power loss. External logic for this functionality is not necessary. If the BIOS remains in the S5 state after AC power loss, only the power button or the RTC alarm can bring the system out of the S5 state. The status of enabled wake events will be lost.

3.7 Power Measurement Support

Power measurement resistors are provided on the platform to measure the power of most subsystems. All power measurement resistors have a tolerance of 1%. The value of these power measurement resistors are 2 mΩ by default. Power on a particular subsystem is calculated using the following formula:

$$P = \frac{V^2}{R}$$

R is the value of the sense resistor (typically 0.002 Ω)

V is the voltage measured across the sense resistor.

It is recommended that the user use a high precision digital multi-meter tool such as the Agilent* 34401A digital multi-meter. Such a meter has 6½ digits of accuracy and can provide a much greater accuracy in power measurement that a common 3½ digit multimeter.

Table 6 summarizes all the power measurement sense resistors located on the 915GM Express Chipset platform. All sense resistors are 0.002 Ω unless otherwise noted.

Table 6. Intel® 915GM® Express Chipset Development Kit Voltage Rails (Sheet 1 of 4)

Voltage Groups	Voltage Rail	Reference Designator
1.0	+V1	U8A2.6
	NC1-6_R	R8A3.2
1.5	+V1.5	Q3J2.1-3
	+V1.5_VCCAUX	R7V1.1
1.5 Always	+V1.5A	R3J12.2
	+V1.5A_ICH	R7V2.1
1.5 Switched	+V1.5S	Q3Y1.1-3
	+V1.5S_DLVDS	R5U15.1
	+V1.5S_TVDAC	C5E3.1
	+V1.5S_DDRDLL	C5R3.1
	+V1.5S_S_PCIE	C5T7.2
	+V1.5S_3GPLL (0.5Ω)	R6R1.1
	+V1.5S_MPLL	C4T1.1
	+V1.5S_HPLL	C4R7.1
	+V1.5S_DPLLA	C5T12.1
	+V1.5S_DPLLB	C5T9.1
	+V1.5S_HMPLL	R4D1.2
	+V1.5S_ICH_EV	R6G10.1
	+V1.5S_PCIE_L	R6G7.2
	+V1.5S_PCIE_ICH	FB6G1.1
	+V1.5S_TVDAC_R2	R5U3.2
	+V1.5S_QTVDAC	C5E2.1
	+V1.5S_ICH	R7H13.2
	+V1.5S_GPLL_ICH	R6V13.2
	+V1.5S_APLL_ICH	R7H8.2
1.8	+VCCA_PROC	R3C4.2
	+V1.8_DDR	R5B11.2
	+V1.8_DIMM	R5B12.2
	+V1.8_LAN	R5B1.2
	+VDDQ_VTTVR	R4N6.2
	DDR_6225_VOUT1 (0.005Ω)	R5B2.2
12.0 Switched	+12S	Q5H2.5-8
	+12S_PCI	R9B2.2
	+V12S_PCIESLOT0	R8B11.2
2.5 Switched	V2.5S	Q2J3.1-3
	V2.5_ALVDS	R5U1.1

Table 6. Intel® 915GM® Express Chipset Development Kit Voltage Rails (Sheet 2 of 4)

Voltage Groups	Voltage Rail	Reference Designator
	V2.5_TXLVDS	R5F6.1
	V2.5_HV	R5U17.2
	V2.5_3GBG	R6E2.2
	V2.5_CRTDAC	C5U2.3
	V2.5_SYNC	R5F7.2
	V2.5_PCI_IDE	R7W9.1
3.3	+V3.3	Q4G2.1-3
	+V3.3_VCCPAUX	R7U2.2
	+V3.3_LPCSLOT	R8F8.2
	+V3.3_LAN	R9A1.2
	+VLAN_18-33	R7A1.1
	+VLAN_33-33	R8B12.1
	+VLAN_10-33	R8N1.1
	+V3.3_PCISLT3	R9B3.2
	+V3.3_ACZ (0Ω)	R8E1.1
3.3 Always	+V3.3A (0.05Ω)	R2H4.2
	+V3.3A_ICH	R7F5.1
	+V3.3A_VCCPAUX	R7U2.2
	+V3.3A_R1_TPM	R9A4.1
	+V3.3A_VCCPSUS	R8F10.2
	+V3.3A_KBC	R8H6.2
3.3 Switched	+V3.3S	Q4G1.1-3
	+V3.3S_TVDAC	R5F6.2
	+V3.3S_TVDACA	C4T10.1
	+V3.3S_TVDACB	C5T18.1
	+V3.3S_TVDACC	C5T17.1
	+V3.3S_AVTBG	C5T14.1
	+V3.3S_PEG	R6C1.2
	+V3.3S_ICH	R8U3.2
	+V3.3S_LVDSBKLT	R6V3.1
	+V3.3S_L	R6E1.2
	+V3.3S_PCI	R9A6.1
	+V3.3S_PCISLOT0	R7C5.2
	+V3.3S_PCISLOT1	R7B20.2
	+V3.3S_PCISLOT2	R8D1.2
	+V3.3S_CLKRC	R5G7.1
	+V3.3S_CLKVDD (2.2Ω)	R5W1.1

Table 6. Intel® 915GM® Express Chipset Development Kit Voltage Rails (Sheet 3 of 4)

Voltage Groups	Voltage Rail	Reference Designator
	+V3.3S_SSCD	R6D1.2
	+V3.3S_BUFFER	R7C6.2
	+V3.3S_DB400	R7C7.2
	+V3.3S_FWH	R8W4.2
	+V3.3S_SIO	R7E7.2
	+V3.3S_IR	R4A3.2
	+V3.3S_R1_TPM	R9M2.2
	+V3.3S_SATA_P2	R6H4.2
	+V3.3S_LVDSDDC	R6V5.2
	+V3.3S_DB400_VDDA	R7C16.2
	VDD_A_CR (2.2Ω)	R5W1.2
	+V3.3S_CLKVDD1 (2.2Ω)	R6W10.1
	VDD_48_CR	R6W10.2
	VDD_REF_CR (1Ω)	R5W4.1
5.0	+5V	Q4V4.1-3
	+5V_LPCSLOT	R8F9.2
	+5V_R1_TPM	R9M1.2
	+5V_VTTVR	R4N1.2
	+5V_PS2	R1B1.1
5.0 Always	+V5A	Q4G4.5-8
	+V5SB_ATXA	R5J4.2
	USBPWR	R3B1.1
	IN_D_R	R6J1.1
5.0 Switched	+5VS	Q4G4.1-3
	+5VS_F_DAC	FB2A2.2
	+5V_PCISLT3	R8B10.2
	+5VS_PATA	R5J3.2
	+5VS_SATA_P2	R7H14.2
	+5VS_PCI	R9B5.1
	+5VS_PHASE1 (CPU Core)	R1B7.2
	+5VS_PHASE2 (CPU Core)	R3B3.2
	+5VS_VTTMCH	R4V1.2
Battery Voltage	+VBAT	U4F2.14
	+VCC_LVDSBKLT	R6F9.1
	VBAT_VTTVR	R4G2.2
	VDC_VDDQVR	R5B5.1
	+VBAT_MCHVR	R4G1.2

Table 6. Intel® 915GM® Express Chipset Development Kit Voltage Rails (Sheet 4 of 4)

Voltage Groups	Voltage Rail	Reference Designator
Batter Voltage Always	+VBATA	R5J1.2
	+V12_ATX	R5J1.1
Battery Voltage Switched	+VBATS	Q6B2.5-8
	+V12S_PEG	R6B5.1
	VBATS_L	R5G1.2
	+V12S_PCISLOT0	R8B11.2
	+V12S_PCISLOT1	R7B19.2
	+V12S_PCISLOT2	R8C6.2
	+V12S_SATA_P2	R7H12.2
	+12VS_PATA	R4X4.2
	+VCC_GMCH_CORE	R4T2.2
	+VCC_GMCH	R4T2.1
	+VCCP	R3T1.2
	+VCCP_GMCH	R4T1.1
	+VCCP_VCCPCPU	R6W7.1
-12	-V12a	R4Y2.2
	-V12A_ATX	R4Y2.1
Battery Charger	+VCHRGR (0.025Ω)	R1H6.2

Hardware Reference 4

This section provides reference information on the hardware, including locations of evaluation board components, connector pinout information and jumper settings. Figure 2 provides an overview of basic board layout.

4.1 Primary Features

Figure 2 shows the major components of the 915GM Express Chipset board and Table 7 gives a brief description of each component.

Figure 2. 915GM Express Chipset Component Locations

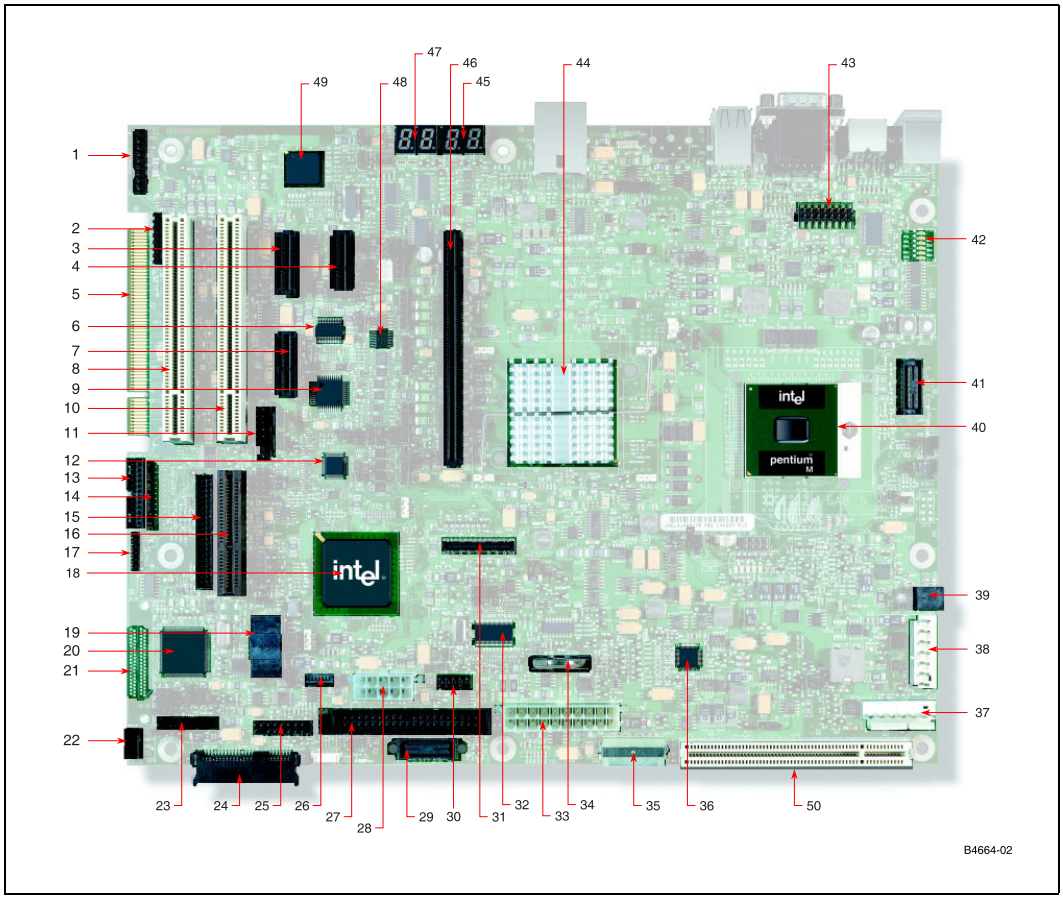


Table 7. 915GM Express Chipset Component Location Legend

1	Reserved	18	Intel ICH6-M	35	Parallel ATA Power
2	Reserved	19	FWH	36	4-in-1 VREG Controller
3	PCI Express Slot 0	20	SMC/KBC	37	Reserved
4	PCI Express Slot 1	21	Reserved	38	Reserved
5	Reserved	22	Reserved	39	AC Brick Connector
6	DB400 Clock Buffer	23	Reserved	40	Intel Processor
7	PCI Express Slot 2	24	SATA Direct Connect	41	XDP Connector
8	PCI Slot 4	25	Front Panel Header	42	VID LEDS
9	Port 80	26	SATA Cable Connect	43	Reserved
10	PCI Slot 3	27	Parallel ATA Connector	44	Intel® 915GM® Express Chipset Development Kit (GMCH)
11	Reserved	28	SATA Power Connector	45	Port 82-83 Display
12	SMSC SIO	29	Reserved	46	PCI Express Graphics Slot
13	Reserved	30	Front Panel USB	47	Port 80-81 Display
14	Keyboard Scan Matrix	31	LVDS Connector	48	CK-SSCD
15	LPC Sideband Header	32	CK_410M	49	LAN Component
16	LPC Slot	33	ATX Power Supply Connector	50	Reserved
17	Reserved	34	RTC Battery		

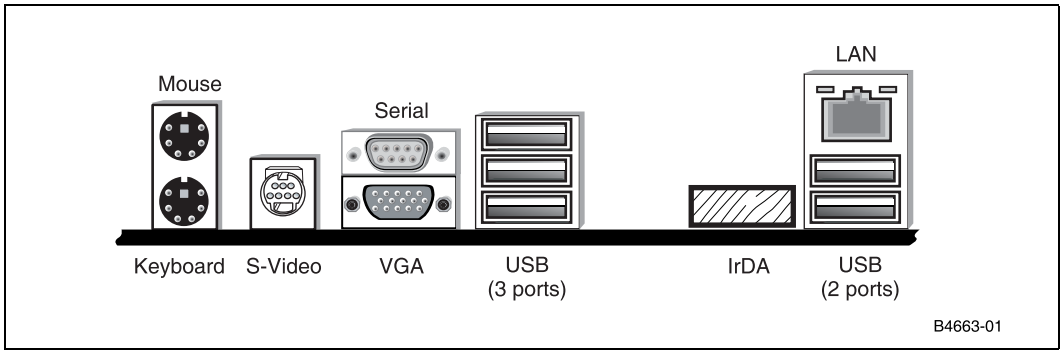
4.2 Back Panel Connectors

Note: Many of the connectors provide operating voltage (+5 V DC and +12 V DC, for example) to devices inside the computer chassis, such as fans and internal peripherals. Most of these connectors are not over-current protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the 915GM Express Chipset panel connectors on the 915GM Express Chipset platform.

Figure 3 shows the back panel connectors to the 915GM Express Chipset platform.

Figure 3. Back Panel Connector Locations



4.3 Configuration Settings

Note: Do not move jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumper settings. Failure to do so may cause damage to the board.

Figure 4 shows the location of the configuration jumpers and switches.

Table 8 summarizes the supported jumpers and switches and gives their default and optional settings.

Table 9 summarizes the unsupported jumpers and switches and gives their default position. The unsupported jumpers must remain in their default position or the operation of the platform is unpredictable. The 915GM Express Chipset board is shipped with the jumpers and switches shunted in the default locations.

Figure 4. Configuration Jumper and Switch Locations

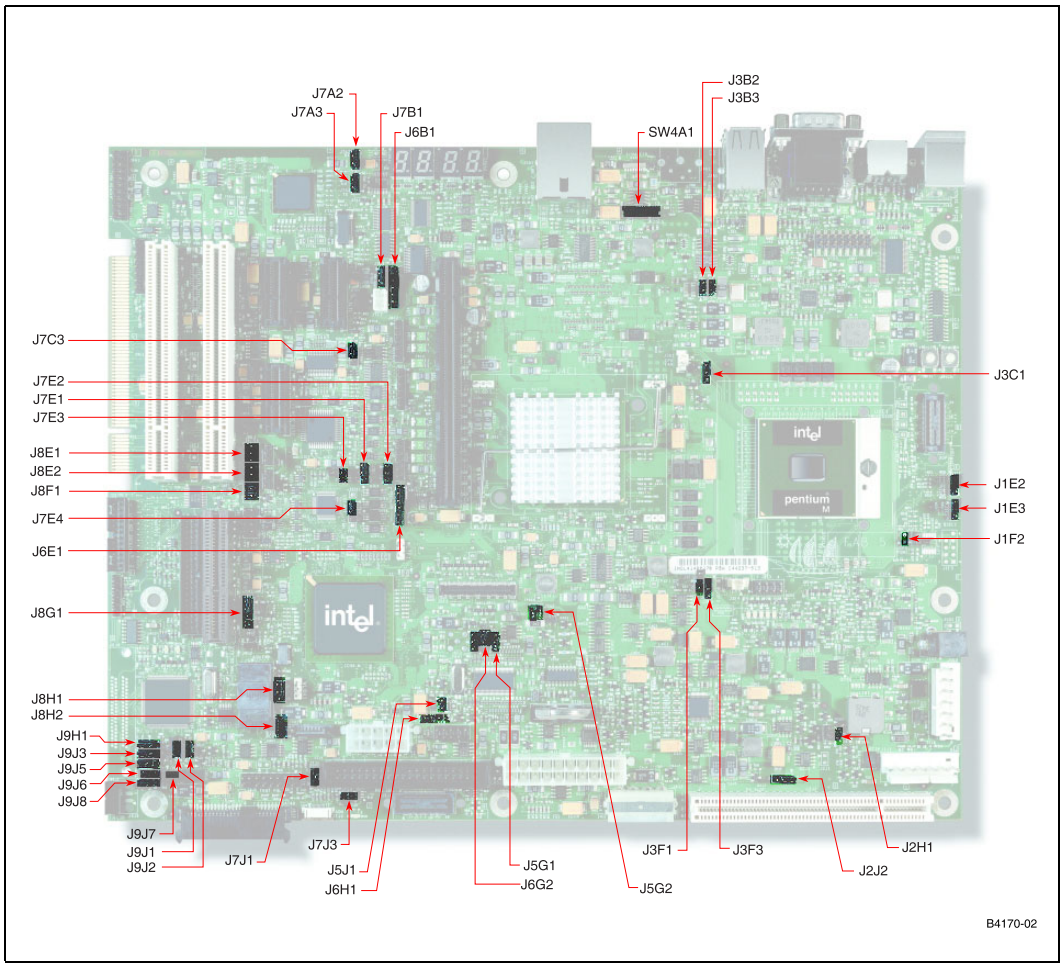


Table 8. Supported Configuration Jumper/Switch Settings

No.	Default Setting	Optional Setting	Option Setting	Ref. Desig.
1	SIO Reset	1-2 Normal Operation	2-3 to hold the SIO in Reset	J7E4
2	H8 Reset	1-2 Normal Operation	2-3 to hold the H8 in Reset	J8G1
3	1 Hz Clock	Out - Normal Operation	IN - Clock disabled- enable H8 Programming	J9G1
4	H8 Programming	OUT - Normal Operation	In - Enable external H8 Programming.	J9J3
5	LID Switch	1-2 Normal Operation	2-3 LID Switch Closed	SW9J2
6	H8 Disable	OUT - Normal Operation	1-2 disable the H8	J9J1
7	BIOS Recovery	OUT - Normal Operation	IN - Recover BIOS	J8H2
8	In-Circuit H8 Programming	1-2 Normal Operation	2-3 to program the H8	J7J1
9	Clear CMOS	OUT - Normal operation	In to clear	J6H1
10	Force Shutdown	OUT - Normal operation	IN to force the board to shutdown.	J2H1
13	Thermal Diode Connection	1-2 Normal Operation	Empty - Disable the processor thermal diode from ADM1023	J3B3
14	Sleep S3 Hot/Cold Switch	1-2 S3_HOT	2-3 S3_COLD	SW4A1
15	Tx Select	1-2 Normal Operation	2-3 connect TxD to H8 for programming	J7A3
16	Rx Select	1-2 Normal Operation	2-3 connect RxD to H8 for programming	J7A2

Table 9. Unsupported Jumper Default Position

Jumper	Pins
J1E2	2-3
J1E3	2-3
J1F2	1-X[1]
J2J2	1-2
J3B3	3-4
J3C1	1-2
J3F1	1-X[1]
J3F3	1-2
J5G1	1-X[1]
J5G2	1-X[1]
J6E1	2-3
J6E1	5-6
J6G2	1-X[1]
J7B1	2-3

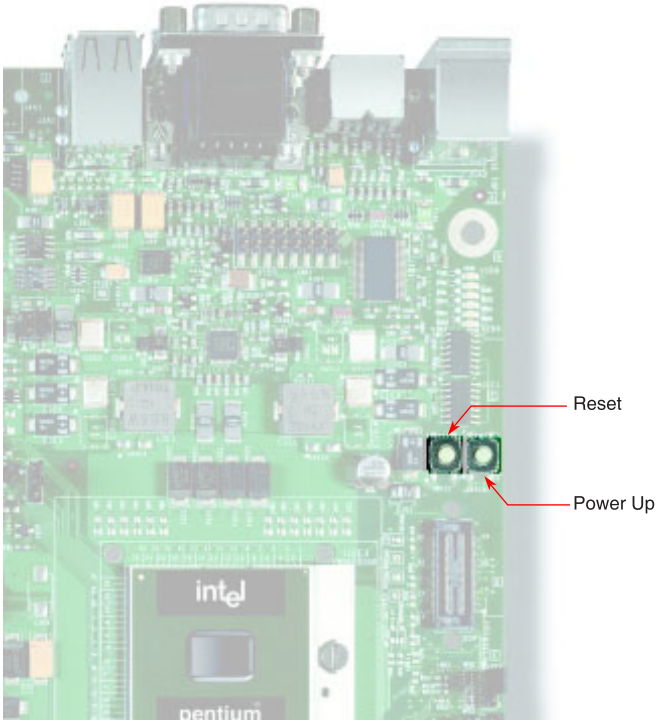
Jumper	Pins
J7C3	1-2
J7E1	1-2
J7E3	1-X[1]
J7J3	1-X[1]
J8E1	2-3
J8E2	2-3
J8F1	1-X[1]
J8H1	2-3
J9J2	1-2
J9J5	1-2
J9J6	1-X[1]
J9J7	1-X[1]
J9J8	1-2
SW4A1	1-2

NOTE:
1. X indicates that the jumper is installed with one contact affixed to pin one and the other contact disconnected.

4.4 Power On and Reset Buttons

The 915GM Express Chipset board has two push buttons, POWER and RESET. The POWER button releases power to the entire board, causing the board to boot. The RESET button will force all systems to warm reset. The two buttons are located near the CPU close to the edge of the board. The POWER button is located at SW1C2 (#1 below) and the RESET button is located at SW1C1 (#2 below).

Figure 5. Intel® 915GM® Express Chipset Development Kit Power On and Reset Buttons



B4728-01

4.5 LEDs

The following LEDs provide status for various functions on the 915GM Express Chipset board.

Table 10. 915GM Express Chipset LED Function Legend

Function	LED
Keyboard Number Lock	CR9G1
Keyboard Scroll Lock	CR9G2
Keyboard Caps Lock	CR9G3
System State S0	CR3G4
System State S3_COLD	CR3G1
System State S3_HOT	CR3G2
System State S4	CR3G3
System State S5	CR2G1
ATA Activity	CR7J1
VID 0	CR1B1
VID 1	CR1B2
VID 2	CR1B3
VID 3	CR1B4
VID 4	CR1B5
VID 5	CR1B6

4.6 Other Headers

4.6.1 H8 Programming Headers

The microcontroller for system management/keyboard/mouse control can be upgraded in two ways. The user can either use a special MS-DOS* utility or use an external computer connected to the system via the serial port on the board.

If the user chooses to use an external computer connected to the system via the serial port, there are five jumpers that have to be set correctly first. Please refer to Table 11 for a summary of these jumpers and refer to Figure 4 for the location of each jumper.

Caution: Make sure the motherboard is not powered on and the power supply is disconnected before moving any of the jumpers.

Here is the sequence of events necessary to program the H8.

1. With the board powered off, move the five jumpers listed in Table 11 to the programming stuffing option.
2. Power the S5 voltage rails by attaching an AC brick or an ATX power supply to the system.

3. Program the H8 via the serial port.
4. Disconnect the power supply from the system.
5. With the board powered off, move the five jumpers listed in Table 11 back to the default stuffing option.

Table 11. H8 Programming Jumpers

#	Jumper	Reference Designator	Default Stuffing Option	Programming Stuffing Option
3	1Hz Clock	J9H1	Out - normal operation - clock enabled	IN - clock disabled - enable H8 programming
4	H8 Programming	J9J3	OUT - normal operation	IN - enable external H8 programming
8	In-circuit H8 Programming	J7J1	1-2 normal operation (SIO)	2-3 connect TxD to H8 for programming
15	Tx Select	J7A3	1-2 Normal Operation	2-3 connect TxD to H8 for programming
16	Rx Select	J7A2	1-2 normal operation (SIO)	2-3 connect RxD to H8 for programming

4.6.2 Expansion Slots and Sockets

Table 12. Expansion Slots and Sockets

Reference Designator	Slot/Socket Description	Detail
U2E1	478 Pin Grid Array (Micro-FCPGA) Processor Socket	
J5N1	DDR2 - Channel A - SODIMM slot	
J5P1	DDR2 - Channel B - SODIMM slot	
J5F1	LVDS Graphics Interface	
J6C1	PCI Express (x16)	Table 13
J6C1	ADD2-R Slot	Table 14
J7C2	PCI Express (x1) Slot 1	Table 15
J8C1	PCI Express (x1) Slot 2	Table 15
J8D1	PCI Express (x1) Slot 3	Table 15
J8B1	PCI 2.3 Slot 1	
J9B3	PCI 2.3 Slot 2	
J7J2	IDE Interface Connector	
J8J3	Mobile SATA Hard Drive Interface Connector	
J7H1	Desk Top SATA Hard Drive Interface Connector	
J6H3	SATA Desk Top Power Connector	
U8G1	Intel Firmware Hub Socket	
BT5H1	Battery	

4.6.2.1 478 Pin Grid Array (Micro-FCPGA) Socket

The pin locking mechanism on the CPU socket is released by rotating the screw on the socket 180 degrees counter-clockwise. CPU pins are keyed so as to only allow insertion in one orientation. DO NOT FORCE CPU into socket. Once the CPU is properly seated into the socket, turn the screw 180 degrees clock-wise to secure the CPU in the socket. Note that the slot on the screw aligns with the lock and unlock legend on the case of the CPU socket.

Caution: Please refer to the CPU installation instruction in Appendix A prior to inserting the CPU as the CPU and socket can be easily damaged.

4.6.2.2 PCI Express (x16)

The platform has one 16 lane PCI Express Graphics slot and supports either x1 or x16 modes. The slot is wired “lane reversed” which connects the 915GM Express Chipsetlanes 0 through 15 to lanes 15 through 0 on the slot. The 915GM Express Chipset will internally un-reverse this wiring since its CFG9 power-on strap is tied low.

Table 13. PCI Express (x16) Pinout (J6C1) (Sheet 1 of 3)

Pin	Description	Pin	Description
A1	PRSNT1#	B1	+12 V
A2	+12 V	B2	+12 V
A3	+12 V	B3	RSVD
A4	GND	B4	GND
A5	(JTAG) TCK	B5	SMCLK
A6	(JTAG) TDI	B6	SMDAT
A7	(JTAG) TDO	B7	GND
A8	(JTAG) TMS	B8	+3.3 V
A9	+3.3 V	B9	(JTAG) TRST#
A10	+3.3 V	B10	+3.3 VAUX
A11	PERST#	B11	WAKE#
A12	GND	B12	RSVD
A13	REFCLK+	B13	GND
A14	REFCLK-	B14	LANE 0 (T+)
A15	GND	B15	LANE 0 (T-)
A16	LANE 0 (R+)	B16	GND
A17	LANE 0 (R-)	B17	PRSNT2*
A18	GND	B18	GND
A19	RSVD	B19	LANE 1 (T+)
A20	GND	B20	LANE 1 (T-)
A21	LANE 1 (R+)	B21	GND
A22	LANE 1 (R-)	B22	GND
A23	GND	B23	LANE 2 (T+)
A24	GND	B24	LANE 2 (T-)

Table 13. PCI Express (x16) Pinout (J6C1) (Sheet 2 of 3)

Pin	Description	Pin	Description
A25	LANE 2 (R+)	B25	GND
A26	LANE 2 (R-)	B26	GND
A27	GND	B27	LANE 3 (T+)
A28	GND	B28	LANE 3 (T-)
A29	LANE 3 (R+)	B29	GND
A30	LANE 3 (R-)	B30	RSVD
A31	GND	B31	PRSNT2#
A32	RSVD	B32	GND
A33	RSVD	B33	LANE 4 (T+)
A34	GND	B34	LANE 4 (T-)
A35	LANE 4 (R+)	B35	GND
A36	LANE 4 (R-)	B36	GND
A37	GND	B37	LANE 5 (T+)
A38	GND	B38	LANE 5 (T-)
A39	LANE 5 (R+)	B39	GND
A40	LANE 5 (R-)	B40	GND
A41	GND	B41	LANE 6 (T+)
A42	GND	B42	LANE 6 (T-)
A43	LANE 6 (R+)	B43	GND
A44	LANE 6 (R-)	B44	GND
A45	GND	B45	LANE 7 (T+)
A46	GND	B46	LANE 7 (T-)
A47	LANE 7 (R+)	B47	GND
A48	LANE 7 (R-)	B48	PRSNT#2
A49	GND	B49	GND
A50	RSVD	B50	LANE 8 (T+)
A51	GND	B51	LANE 8 (T-)
A52	LANE 8 (R+)	B52	GND
A53	LANE 8 (R-)	B53	GND
A54	GND	B54	LANE 9 (T+)
A55	GND	B55	LANE 9 (T-)
A56	LANE 9 (R+)	B56	GND
A57	LANE 9 (R-)	B57	GND
A58	GND	B58	LANE 10 (T+)
A59	GND	B59	LANE 10 (T-)
A60	LANE 10 (R+)	B60	GND
A61	LANE 10 (R-)	B61	GND
A62	GND	B62	LANE 11 (T+)

Table 13. PCI Express (x16) Pinout (J6C1) (Sheet 3 of 3)

Pin	Description	Pin	Description
A63	GND	B63	LANE 11 (T-)
A64	LANE 11 (R+)	B64	GND
A65	LANE 11 (R-)	B65	GND
A66	GND	B66	LANE 12 (T+)
A67	GND	B67	LANE 12 (T-)
A68	LANE 12 (R+)	B68	GND
A69	LANE 12 (R-)	B69	GND
A70	GND	B70	LANE 13 (T+)
A71	GND	B71	LANE 13 (T-)
A72	LANE 13 (R+)	B72	GND
A73	LANE 13 (R-)	B73	GND
A74	GND	B74	LANE 14 (T+)
A75	GND	B75	LANE 14 (T-)
A76	LANE 14 (R+)	B76	GND
A77	LANE 14 (R-)	B77	GND
A78	GND	B78	LANE 15 (T+)
A79	GND	B79	LANE 15 (T-)
A80	LANE 15 (R+)	B80	GND
A81	LANE 15 (R-)	B81	PRST2#
A82	GND	B82	RSVD

4.6.2.3 ADD2 Slot

When not being used for PCI Express, the x16 slots can be used for Serial Digital Video Out (SDVO), which is also sometimes referred to as ADD2 (Advanced Digital Display 2nd generation). SDVO cards provide for a third party vendor secondary graphics add-on such as a digital panel interface. It is important to note that the 915GM Express Chipset does not support lane reversal of its SDVO interface and since the slot is routed lane reversed, a special SDVO card which un-reverses the lanes must be used. These cards are sometimes referred to as ADD2-R (“R” for reversed) cards.

Note: ADD2-N (“N” for normal) cards are not compatible with the board.

Table 14. ADD2 Slot (J6C1) (Sheet 1 of 4)

Pin Number	A	B
1	N/C	12 V
2	12 V	12 V
3	12 V	Reserved
4	GND	GND
5	N/C	N/C
6	N/C	N/C

Table 14. ADD2 Slot (J6C1) (Sheet 2 of 4)

Pin Number	A	B
7	N/C	GND
8	N/C	3.3 V
9	3.3 V	N/C
10	3.3 V	N/C
11	RESET	N/C
Key		
12	GND	Reserved
13	N/C	GND
14	N/C	SDVOC_Red+
15	GND	SDVOC_Red-
16	SDVOC_TV_CLK_In+	GND
17	SDVOC_TV_CLK_In-	SDVO_CtrlClk
18	GND	GND
End of x1 Connector		
19	Reserved	SDVOB_Green+
20	GND	SDVOB_Green-
21	SDVOB_Int+	GND
22	SDVOB_Int-	GND
23	GND	SDVOB_Blue+
24	GND	SDVOB_Blue-
25	SDVOB_Stall+	GND
26	SDVOB_Stall-	GND
27	GND	SDVOB_Clk+
28	GND	SDVOB_Clk-
29	N/C	GND
30	N/C	Reserved
31	GND	SDVOB_CtrlData
32	Reserved	GND
End of x4 Connector		
33	Reserved	SDVOC_Red+
34	GND	SDVOC_Red-
35	N/C	GND
36	N/C	GND
37	GND	SDVOB_Green+
38	GND	SDVOB_Green-
39	SDVOB_Int+	GND
40	SDVOB_Int-	GND
41	GND	SDVOB_Blue+

Table 14. ADD2 Slot (J6C1) (Sheet 3 of 4)

Pin Number	A	B
42	GND	SDVOB_Blue-
43	N/C	GND
44	N/C	GND
45	GND	SDVOB_Clk+
46	GND	SDVOB_Clk-
47	N/C	GND
48	N/C	N/C
49	GND	GND
End of x8 Connector		
50	Reserved	N/C
51	GND	N/C
52	N/C	GND
53	N/C	GND
54	GND	N/C
55	GND	N/C
56	N/C	GND
57	N/C	GND
58	GND	N/C
59	GND	N/C
60	N/C	GND
61	N/C	GND
62	GND	N/C
63	GND	N/C
64	N/C	GND
65	N/C	GND
66	GND	N/C
67	GND	N/C
68	N/C	GND
69	N/C	GND
70	GND	N/C
71	GND	N/C
72	N/C	GND
73	N/C	GND
74	GND	N/C
75	GND	N/C
76	N/C	GND
77	N/C	GND
78	GND	N/C

Table 14. ADD2 Slot (J6C1) (Sheet 4 of 4)

Pin Number	A	B
79	GND	N/C
80	N/C	GND
81	N/C	N/C
82	GND	Reserved

4.6.2.4 PCI Express (x1)

The three PCI Express x1 connectors allow the use of any industry standard PCI Express device. The pin configuration of the connectors is given below.

Table 15. PCI Express (x1) Pinout (J7C2, J8C1 & J8D1)

Pin	Description	Pin	Description
A1	PRSNT1#	B1	+12 V
A2	+12 V	B2	+12 V
A3	+12 V	B3	RSVD
A4	GND	B4	GND
A5	(JTAG) TCK	B5	SMCLK
A6	(JTAG) TDI	B6	SMDAT
A7	(JTAG) TDO	B7	GND
A8	(JTAG) TMS	B8	+3.3 V
A9	+3.3 V	B9	(JTAG) TRST#
A10	+3.3 V	B10	+3.3 VAUX
A11	PERST#	B11	WAKE#
A12	GND	B12	RSVD
A13	REFCLK+	B13	GND
A14	REFCLK-	B14	LANE 0 (T+)
A15	GND	B15	LANE 0 (T-)
A16	LANE 0 (R+)	B16	GND
A17	LANE 0 (R-)	B17	PRSNT2*
A18	GND	B18	GND

4.6.2.5 IDE Connector

Table 16. IDE Connector (J7J2)

Pin	Signal	Pin	Signal
1	Reset IDE	2	Ground
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	Ground	20	Key
21	DRQ3	22	Ground
23	I/O Write	24	Ground
25	I/O Read	26	Ground
27	I/O Ch Ready	28	CSEL
29	DACK 3	30	Ground
31	IRQ 14	32	NC
33	Address 1	34	DATA Detect
35	Address 0	36	Address 2
37	Chip Select 0	38	Chip Select 1
39	Activity	40	Ground

4.6.2.6 SATA Pinout

Table 17. SATA Pinout (J7H1)

Pin	Signal
1	GND
2	TXP
3	TXN
4	GND
5	RXN
6	RXP
7	GND

Table 18. SATA Port 2 Power Connector Pinout (J6H3)

Pin	Signal
1, 2	+3.3 V
3, 4	+5 V
5	+12 V
6, 7, 8, 9, 10	GND

Table 19. SATA Port 0 Mobile Drive Connector Pinout (J8J3)

Pin	Signal
2	TX
3	TX#
5	RX
6	RX#
8, 9, 10	+3.3 V
14, 15, 16, 18	+5 V
20, 21, 22	+12 V
1, 4, 7, 11	GND
12, 13, 17, 19	GND

4.6.2.7 Fan Connectors

Table 20. Fan Connectors (J3F4 and J3B1)

Pin	Signal
1	+5V
2	GND

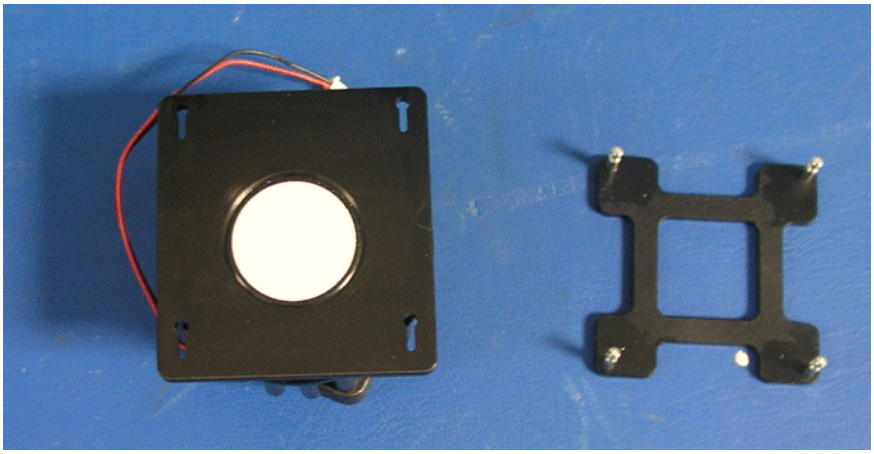
Heat Sink Installation Instructions A

It is necessary for the Mobile Intel® 915GM® Express Chipset to have a thermal solution attached to the processor in order to keep the processor within its operating temperature.

A heat sink is included in the kit. To install the heat sink:

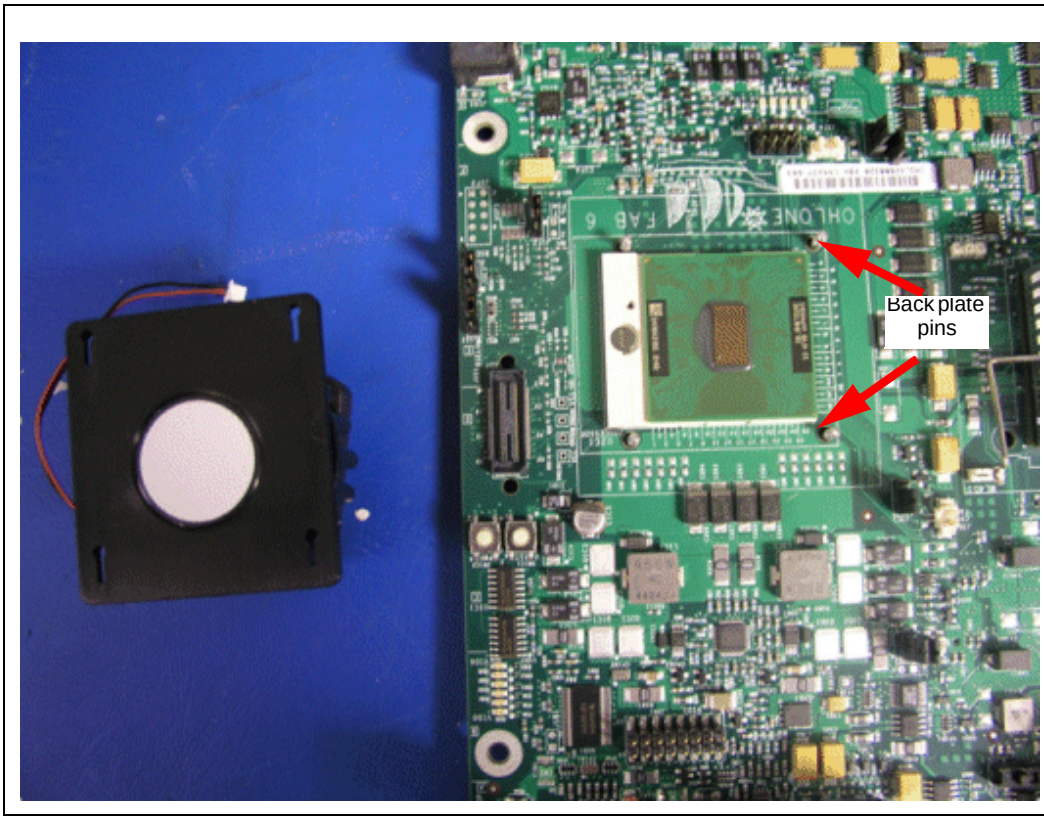
1. Remove heat sink from its package and separate the fan sink portion from the heat sink back plate.

Figure 6. Heat Sink and Back Plate



2. Examine the base of the heat sink, where contact with the processor die is made. There is a white Thermal Interface Material (TIM) on the surface. Do not add any additional TIMs on top of this white material.
3. Place the back plate on the underside of the board so that the pins protrude through the holes in the system board around the processor.

Figure 7. Back Plate Pins



4. Clean the die of the processor with isopropyl alcohol before the heat sink is attached to the processor. This ensures that the surface of the die is clean.
5. Place the heat sink over the pins of the heat sink back plate. Slide the heat sink over the lugs on the back plate pins so that the base is directly over the processor die. Turn the heat sink clockwise until it contacts the die. Then turn the heat sink ¼ turn to tighten it. The heat sink should be snug but not tight.

Caution: Overtightening the heat sink could cause excessive pressure on the die and damage the processor.

6. Plug the fan connector for the heat sink onto the CPU fan header on the motherboard.

Figure 8. CPU Fan Header

